**Software Requirements Specification (SRS)**

For projects

**1526**

Version: 1.0

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**Table of Contents**

[1 Changes 3](#_Toc503271173)

[2 *Project 1526*: 4](#_Toc503271174)

[2.1 Introduction: 4](#_Toc503271175)

[2.2 System block diagram 4](#_Toc503271176)

[2.3 Objective 5](#_Toc503271177)

[2.4 Synthesizer registers values 5](#_Toc503271178)

[3 Hardware 6](#_Toc503271179)

[3.1 MCU Schematic 6](#_Toc503271180)

[3.2 Microcontroller 7](#_Toc503271181)

[3.3 GPIO and Analog Pin Assignments 7](#_Toc503271182)

[4 Appendix A – How to set the registers values of sensitizer ADF-4351 8](#_Toc503271183)

# Changes

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Change | Version | Date |
| Roee Zinoue | First Edition. | 1.0 | 07/01/18 |

# 

# Project 1526:

## Introduction:

This document describes the SW operation of the SFC unit.

The SFC main goal is to output two signals frequencies at frequency of:

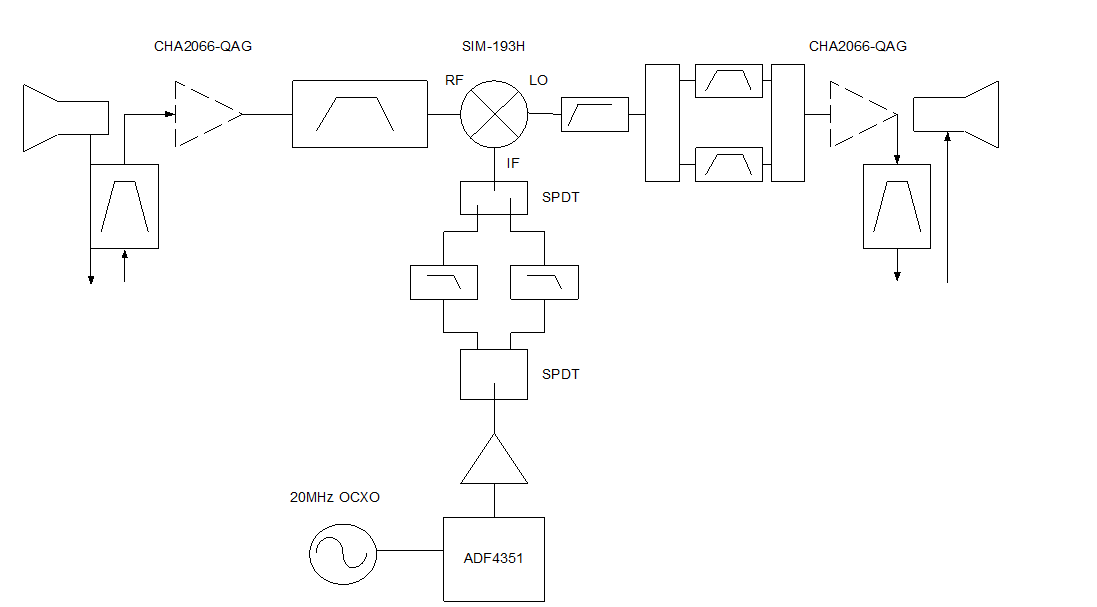
1. 1.95 GHz.
2. 2.8 GHz.

This achieved by written digital configuration words that exit from on board MCU (PIC16LF1823) and already stored by the MCU to synthesizer (ADF-4351) unit.

The system user will able to choose the desire output frequency signal by external switch that connected to the MCU.

The MCU will also have LEDs indication of the synthesizer operation (that indicate about the frequency that selected and if the frequency is latched). The opposite results of the above can also be viewed by 2 GPIO that exit from the MCU.

## System block diagram



## Objective

Main object of the MCU is two configure synthesizer ADF-4351 to output 2 frequencies RF signals at frequencies: a. 1.95 GHz b. 2.8 GHz according to user selection.

Beside that the system will able to:

1. Operate immediate after system power on or system reset. (In case of system boot failure the LEDs will blinks which in a way that it indicate an issue to the system user).
2. Will indicate to the system user the state of synthesizer mode (if the output RF signal is latched or there is an issue in the synthesizer unit).
3. Will output the synthesizer values by 2 GPIO pins that are connected to the MCU.

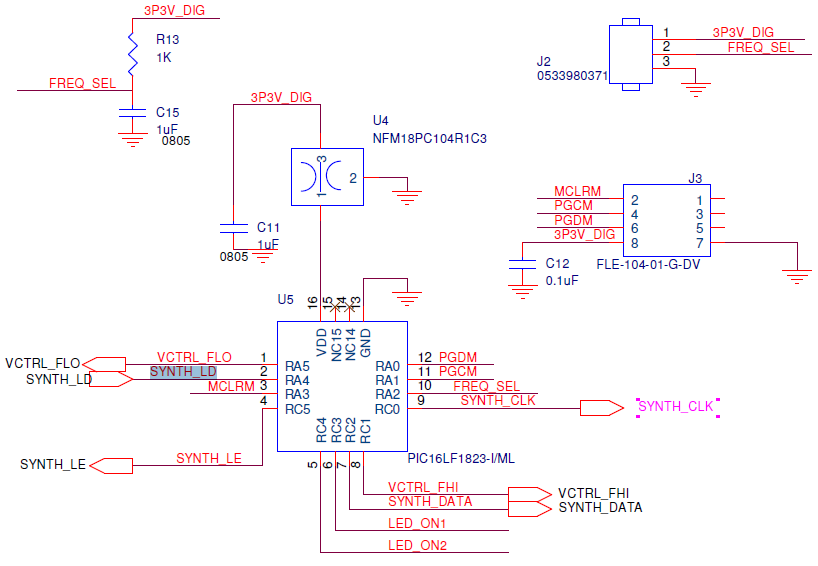
## Synthesizer registers values

Note: Please check [Appendix A](#_Appendix_A_–) on this document describe to learn about the way of frequency in the sensitizer unit.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Register name | Register possible data range | Register data value | | Register bits size |
|  |  |
| FRAQ |  | TBD | TBD | 12 |
| Prescaler (PR1) | 0: 4/5 prescaler  1: 8/9 prescaler | TBD | TBD | 1 |
| INT |  | TBD | TBD | 16 |
| MOD |  | TBD | TBD | 12 |
| D (Reference Doubler) – multiple by 2 REFIN value | 0: disable.  1: Enable. | TBD | TBD | 1 |
| T (reference divide-by-2 bit) |  | TBD | TBD | 1 |
| R (reference division factor) |  | TBD | TBD | 10 |

# Hardware

## MCU Schematic



## Microcontroller

|  |  |
| --- | --- |
| **Recommended PIC** | **PIC16LF1823 – 8 bit core** |
| **Operating voltage** | **3.3V** |
| **Inputs (TTL / converter)** | **TBD** |
| **Outputs (TTL / converter)** | **TBD** |
| **POR** | **Available** |
| **Internal clock** | **8MHz and up to 32MHz** |
| **Pin count** | **14** |

* Flash Memory
  + The PIC microcontroller has 3.5KB (2K x 14) of internal flash memory. This memory will be used for store the internal synthesizer registers data.
* RAM Memory
  + The PIC microcontroller has 128 bytes of internal RAM, the system will use this memory for its software stack & heap.
* Peripherals support:
* Connectivity: 1-UART, 1-SPI, 1-I2C1-MSSP(SPI/I2C).
* ADC: 8 ch, 10-bit.

## GPIO and Analog Pin Assignments

|  |  |  |  |
| --- | --- | --- | --- |
| **Name in document** | **PIN Name** | **Net Name** | **Type** |
| **MCU power and programing pins** | | | |
| **3.3 VDC Enable** | **VDD** | **VDD** | **Input Analog** |
| **Digital ground** | **GND** | **GND** | **Input Analog** |
| **Program data Enable** | **RA0** | **PGDM** | **Bi-directional Discrete** |
| **Program clock Enable** | **RA1** | **PGCM** | **Input Discrete** |
| **System reset** | **RA3** | **MCLRM** | **Input Discrete** |
| **synthesizer** | | | |
| **SYNTH\_CLK** | **RC0** | **SYNTH\_CLK** | **Output Discrete** |
| **SYNTH\_LE** | **RC5** | **SYNTH\_LE** | **Output Discrete** |
| **SYNTH\_LD** | **RA4** | **SYNTH\_LD** | **Input Discrete** |
| **SYNTH\_DATA** | **RC2** | **SYNTH\_DATA** | **Output Discrete** |
| **System indication** | | | |
| **VCTRL\_FHI** | **RC1** | **VCTRL\_FHI** | **Output Discrete** |
| **VCTRL\_FLO** | **RA5** | **VCTRL\_FLO** | **Output Discrete** |
| **LED\_ON1** | **RC3** | **LED\_ON1** | **Output Discrete** |
| **LED\_ON2** | **RC4** | **LED\_ON2** | **Output Discrete** |
| **User selection** | | | |
| **FREQ\_SEL** | **RA2** | **FREQ\_SEL** | **Input Discrete** |

# Appendix A – How to set the registers values of sensitizer ADF-4351

\*\* Please refer to unit datasheet for full details.

The Sensitizer ADF-4351 is software programmable unit which mean that each of the unit registers data is given and controlled by 4 registers that each one have control buffer of 32-bit. This registers configuration values will output from the on board MCU unit.

The synthesizer is also calibrated by the VCO (voltage controlled oscillator) and the frequency that comes after the VCO circuit can be calculated using the formula:

When:

RFOUT: is the output frequency of the voltage controlled oscillator (VCO).

INT: is the preset divide ratio of the binary 16-bit counter.

FRAC: is the numerator of the fractional division (0 to MOD − 1).

MOD: is the preset fractional modulus (2 to 4095).

fPEF: is a frequency parameter that calculated from inputs parameters:

When:

REFIN: is the reference input frequency.

D: is the REFIN doubler bit (0 or 1).

R: is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).

T: is the REFIN divide-by-2 bit (0 or 1).

**Example of frequency calculation:**

As an example, a UMTS system requires a 2112.6 MHz RF frequency output (RFOUT); a 10 MHz reference frequency input (REFIN) is available and a 200 kHz channel resolution (fRESOUT) is required on the RF output.

Note that the ADF4351 VCO operates in the frequency range of 2.2 GHz to 4.4 GHz. Therefore, the RF divider of 2 should be used (VCO frequency = 4225.2 MHz, RFOUT = VCO frequency/ RF divider = 4225.2 MHz/2 = 2112.6 MHz).

It is also important where the loop is closed. In this example, the loop is closed before the output divider (see Figure 30). fPFD PFD VCO N DIVIDER ÷2 RFOUT 09800-027 Figure 30.

Loop Closed before output Divider Channel resolution (fRESOUT) of 200 kHz is required at the output of the RF divider.

Therefore, the channel resolution at the output of the VCO (fRES) needs to be

2 × fRESOUT,

that is, 400 kHz. MOD = REFIN/fRES MOD = 10 MHz/400 kHz = 25 From Equation 4, fPFD = [10 MHz × (1 + 0)/1] = 10 MHz (5) 2112.6 MHz = 10 MHz × [(INT + (FRAC/25))/2] (6) where: INT = 422. FRAC = 13.